EXACT SYNTHESIS OF INTERSTAGE MATCHING NETWORKS FOR BROADBAND MICROWAVE GaAs FET AMPLIFIERS*

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Abstract

The exact synthesis of distributed interstage matching networks for broadband microwave GaAs FET amplifiers is presented. The results presented are based on distributed models of the FET and the design is exact for both maximally-flat and equiripple tapered-magnitude gain characteristics with arbitrary gain slopes.

Introduction

The design of interstage matching networks for broadband microwave GaAs FET amplifiers requires the synthesis of broadband matching networks which will provide 1) compensation for the prescribed gain slope of the transistors, 2)broadband matching to equalize the simultaneous reactive constraints of the transistors, and 3) broadband impedance transformation without transformer. For the interstage matching networks, it is necessary to distribute the zeroes of the reflection coefficients to satisfy the simultaneous reactive constraints imposed by the FETs. In addition, for the design of microwave broadband GaAs FET amplifiers, it is highly desirable to use synthesis techniques directly in the distributed domain. For bandwidth of an octave or above, the conversion of lumped element prototype design to transmission-line realization will often alter drastically the characteristics of the original design.

Based on the distributed models of the GaAs FETs, the exact synthesis of distributed matching networks for broadband microwave GaAs FET amplifiers is presented. The distributed matching networks to be considered in this paper are commensurate transmission-line networks with an arbitrary number of cascade lines and open- and short-ciucuited stubs. The work reported in this paper can be considered as extensions and generalizations of several previous contributions on the design of broadband transistor amplifiers.[1-5]

Broadband Cascaded GaAs FET Amplifiers

The basic two-stage broadband cascaded GaAs FET amplifier configuration is shown in Figure 1. Two of these amplifier modules can be combined by quadrature hybrids to obtain a high-gain and well matched FET amplifier as shown in Figure 2.

For the single-stage amplifier, it is assumed that the transistor is unilateral. For the design of the interstage matching networks, it has been found that this assumption will lead to unacceptable gain variation in the passband. We have used the techniques of remodeling the equivalent circuits to take into account the effects of the nonzero s_{12} of the FETs.

The distributed equivalent circuits for a microwave GaAs FET input and output models are presented in Fig. 3. Based on the measured scattering parameters of the FET, the distributed equivalent circuits are derived. To illustrate this procedure, consider a 1μ-gate GaAs FET discussed by Liechti and Tillman.[6] The input equivalent circuit is given by Figure 3(a) with the element values of $Z_i = 21.998\Omega$ for $\ell = \lambda/8$ at 14GHz and $R_i = 9.704\Omega$. The output equivalent circuit is given by Figure 3(b) with the element values of $Z_o = 148.34\Omega$ for $\ell = \lambda/8$ at 14GHz and $R_o = 501.6\Omega$. These element values are derived using s_{11} and s_{22} for the octave band from 7GHz to 14 GHz and will be modified later to account for s_{12}.

The optimum gain-bandwidth limitations for distributed matching networks have been derived.[7] These ideal limitations can be used to determine the distribution of gain slopes among the input, output, and the interstage matching networks. For the FET under consideration, an ideal zero slope input network requires a flat loss of 0.66 dB while a flat loss of 0.19 dB would be required for an ideal zero slope output matching network. For the interstage matching network, simultaneous reactive constraints must be satisfied for a given gain slope. In addition, it must provide broadband impedance transformation.

The basic structure of the distributed matching networks is an arbitrary cascade of unit elements (UE's) and commensurate open- or short-circuited series and shunt stubs. The gain function of this general class of distributed networks in terms of the Richards' transformation variable Ω is given by

$$G_M(\Omega^2) = \frac{K\Omega^{2m}(1+\Omega^2)^q}{P_n(\Omega^2)} = \frac{Kx^m(1+x)^q}{P_n(x)} \tag{1}$$

where

$\Omega = \tan \omega\tau$ (2)
τ=delay length of the commensurate lines
$x=\Omega^2$
m=number of high-pass sections
q=number of cascade UEs
K=gain constant

In (1), $P_n(x)$ is an nth-order polynomial which will be derived to provide an maximally-flat or equiripple approximation to the ideal tapered-magnitude gain function for the distributed case given by

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$$G_I(x) = \{ \frac{1}{\omega_h \tau} \tan^{-1} \sqrt{x} \}^{2\alpha} \tag{3}$$

where α is the gain taper parameter and ω_h is the radian frequency at the high end of the frequency band. Note that (3) is the ideal gain taper characteristic in the real frequency variable ω. Since commensurate transmission line networks are periodic, for the tapered-magnitude gain functions, the line length must be strictly less than quarter-wavelength at ω_h. The ideal tapered gain characteristic and frequency variables for distributed matching networks are shown in Figure 4.

Two typical interstage matching networks are presented in Figures 5 and 6. For the configuration shown in Figure 5, N = 6, N_L = 2, N_H = 2, and N_C =2 and for the network in Figure 6, N_L = 1, N_H = 2, and N_C = 3. To illustrate the explicit results for an equiripple matching network with a gain slope of 8 dB/octave, consider the circuit in Figure 5 for an octave bandwidth with a gain reduction of 0.5 dB. The element values are given by

Z_{01}=8.4117, Z_{02}=15.3948, Z_{03} =1.4144,
Z_{04}=4.1631, Z_{05}=11.8628, Z_{06}=5.9699,
R=14.1257

We must distribute the zeroes of the reflection coefficients to satisfy the simultaneous reactive constraints imposed by the FET. For the low-pass and the high-pass constraints, simple relationships can be derived to determine the effects of the zero distributions

A two-stage GaAs FET amplifier has been designed and is shown in Figure 7. The initial design is based on a input matching network with 2 dB/octave gain slope, an interstage matching network with 8 dB/octave slope, and an output matching network with 2 dB/octave. The input matching network is N=6, N_L=1, N_H=2, and N_C=3, with no gain reduction and ripple of 0.23 dB. The interstage network is of the same configuration but the gain reduction is 0.5 dB and ripple of 0.75 dB and the zeroes of the reflection coefficient are distributed to absorb both the input and output constraints of the FET. The output matching network is a simple N=4, N_L=1, N_H=1, N_C=2 network with no gain reduction and a ripple of 0.28 dB. The relatively high order and gain slope are necessary for the interstage network to satisfy the gain-bandwidth limitations. In addition, it is found that remodelling of the equivalent circuits are needed to take into account the effects of nonzero s_{12} of both transistors.

The element values presented in Figure 7 are for an optimized two-stage amplifiers. The optimized gain response are tabulated as follows:

Freq. (GHz)	Opt. Gain (dB)
7	13.8
8	14.2
9	13.9
10	13.7
11	14.3
12	14.0
13	13.9
14	14.0

The optimized gain is 14 dB with a maximum variation of $\pm$ 0.3 dB.

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100 TRL AA SE       25.18      56.26  14000.00
110 SST BB PA     -143.47      42.14  14000.00
120 TRL CC SE      -97.12      45.88  14000.00
130 OST DD PA       30.65      39.57  14000.00
140 TRL EE SE      101.16     -47.32  14000.00
150 SST FF PA       82.94     -51.67  14000.00
160 TWO GG S1       50.00
170 OST HH PA   100000.00      45.00  14000.00
180 TRL II SE      100.00      80.20  14000.00
190 TRL JJ SE      -25.86      55.85  14000.00
200 SST KK PA      115.09      50.76  14000.00
210 TRL LL SE      100.00      52.21  14000.00
220 SST MM PA       37.25      55.95  14000.00
230 EQU NN GG
240 SST OO PA   100000.00      45.00  14000.00
250 TRL PP SE      100.00     -61.96  14000.00
260 TRL QQ SE      -28.43      44.93  14000.00
270 SST RR PA      -70.74      37.62  14000.00
280 CAX AA RR
290 PRI AA S1       50.00
300 END
310 7000 14000 1000
320 END
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Scattering Parameters of FET

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330 .826 -88.9 1.69 100.5 .0358 37.4 .834 -19.3
340 .805 -96.5 1.56 92.6 .0375 33.2 .830 -21.4
350 .787 -103.1 1.44 85.2 .0389 29.7 .828 -23.6
360 .771 -108.9 1.34 78.3 .0399 26.6 .826 -25.7
370 .759 -114.1 1.25 71.8 .0407 23.9 .826 -27.8
380 .748 -118.6 1.16 65.6 .0412 21.5 .826 -29.9
390 .739 -122.7 1.09 59.7 .0416 19.4 .827 -31.9
400 .731 -126.3 1.03 54.1 .0419 17.5 .829 -34.0
410 END
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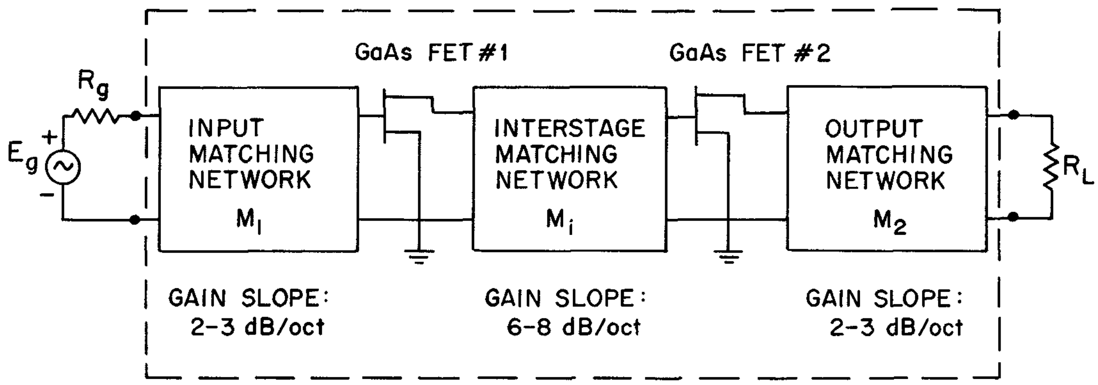
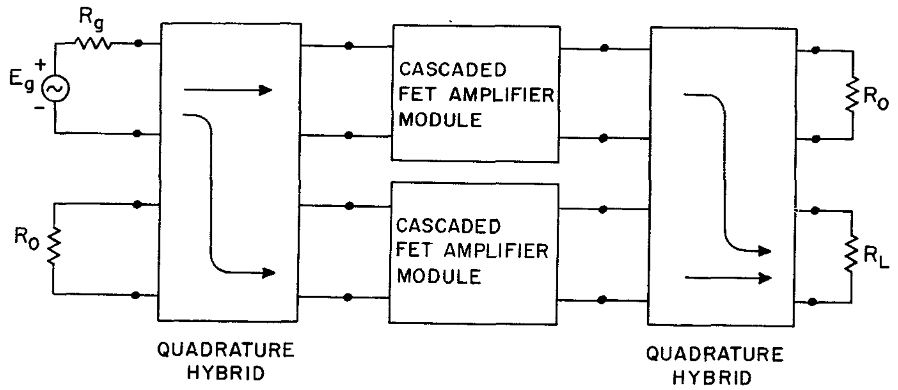


CASCADED FET AMPLIFIER MODULE

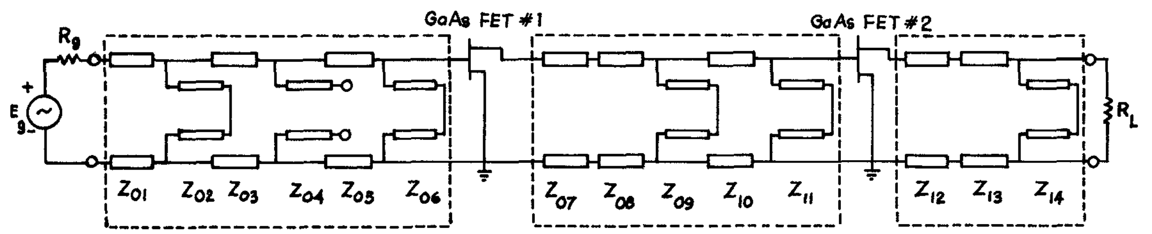
Figure 1



BALANCED HIGH-GAIN FET AMPLIFIER

Figure 2

CASCADED GaAs FET AMPLIFIER



INPUT MATCHING NETWORK

$Z_{01} = 25\Omega$, $\ell_1 = 56°$
$Z_{02} = 144\Omega$, $\ell_2 = 42°$
$Z_{03} = 97\Omega$, $\ell_3 = 46°$
$Z_{04} = 31\Omega$, $\ell_4 = 40°$
$Z_{05} = 101\Omega$, $\ell_5 = 47°$
$Z_{06} = 83\Omega$, $\ell_6 = 52°$

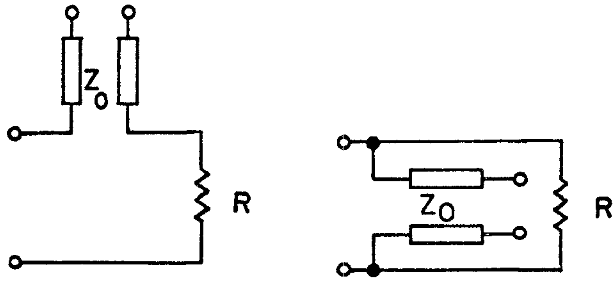
INTERSTAGE MATCHING NETWORK

$Z_{07} = 100\Omega$, $\ell_7 = 80°$
$Z_{08} = 26\Omega$, $\ell_8 = 56°$
$Z_{09} = 115\Omega$, $\ell_9 = 51°$
$Z_{10} = 100\Omega$, $\ell_{10} = 52°$
$Z_{11} = 37\Omega$, $\ell_{11} = 56°$

OUTPUT MATCHING NETWORK

$Z_{12} = 100\Omega$, $\ell_{12} = 62°$
$Z_{13} = 28\Omega$, $\ell_{13} = 45°$
$Z_{14} = 71\Omega$, $\ell_{14} = 38°$

Figure 7



(a) (b)

Figure 3

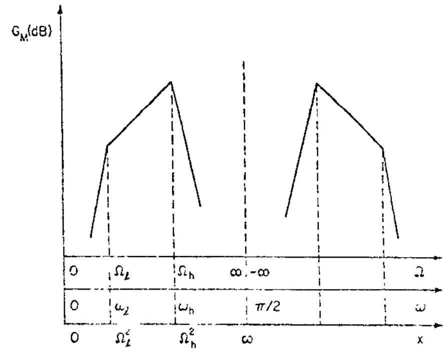


Figure 4

INTERSTAGE MATCHING NETWORK

$N = 6, \quad N_L = 2, \quad N_H = 2, \quad N_C = 2$

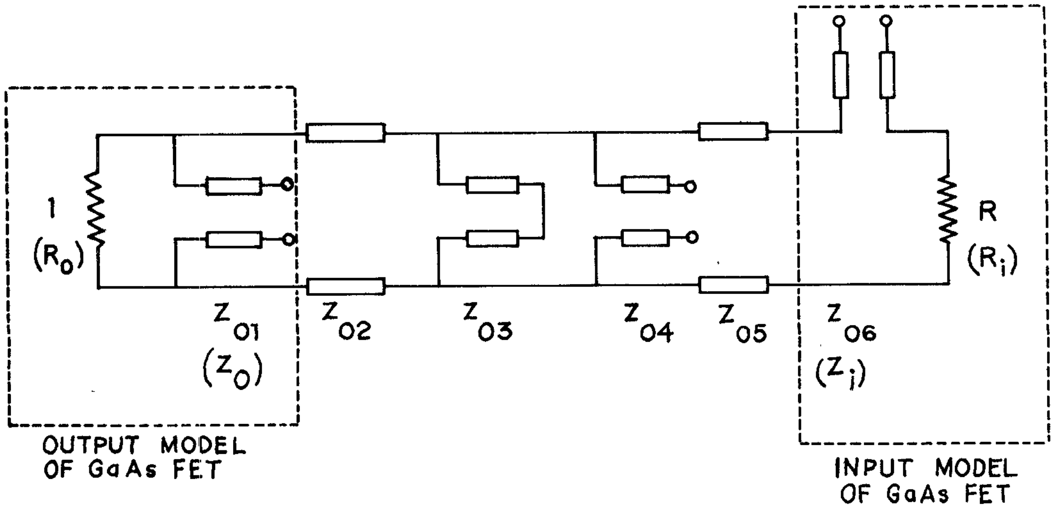


Figure 5

INTERSTAGE MATCHING NETWORK

$N = 6, \quad N_L = 1, \quad N_H = 2, \quad N_C = 3$

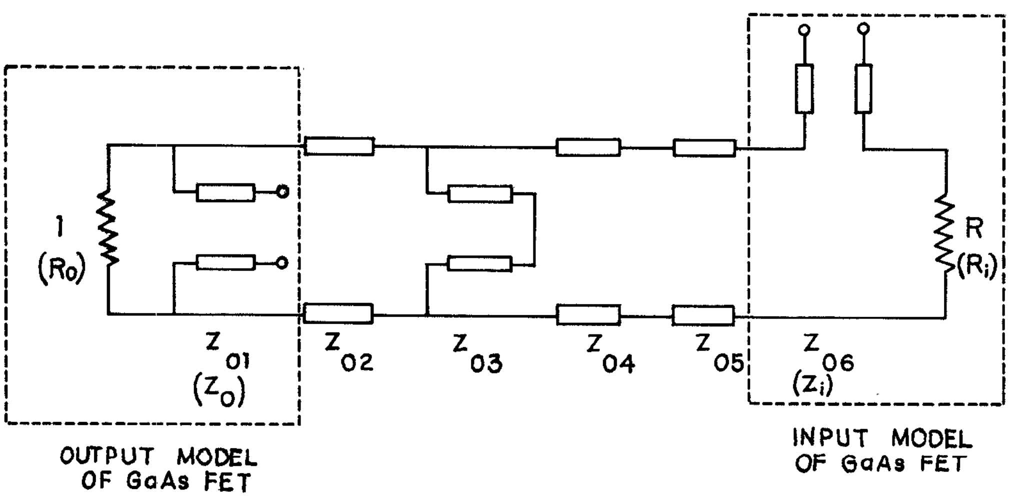


Figure 6